Nanomaterials

DOI: 10.1002/ange.201306086

Critical Crystal Growth of Graphene on Dielectric Substrates at Low Temperature for Electronic Devices**

Dacheng Wei, Yunhao Lu, Cheng Han, Tianchao Niu, Wei Chen, and Andrew Thye Shen Wee**

Graphene is regarded as one of the most promising candidate materials for future electronics.[1–4] For usage in electrical devices, high-quality graphene needs to be placed on a dielectric surface. Currently, methods for graphene preparation require graphene to be transferred from scotch tape,[2] metals,[3] or solutions[4] to the dielectric substrate for electrical applications. The transfer process normally induces contamination, wrinkles, or even breakage of the graphene samples and thus hampers the practical application of graphene in electronics.[3] Moreover, chemical vapor deposition (CVD) on a metal catalyst normally requires a growth temperature as high as 800–1000 °C. For industrial-scale production, low-temperature growth can lead to a decrease in energy consumption and cost, and an increase in compatibility. Therefore, a low-cost, controllable, and reliable method is required for the production of clean high-quality graphene directly on dielectric substrates at low temperature. One pioneering study towards the goal of the catalyst-free growth of graphene on dielectric materials examined the pyrolysis of CH_4 on bare SiO_2/Si;[5,6] however, this method requires a high growth temperature (1100–1650 °C). Another approach, plasma-enhanced CVD (PECVD), enables the low-temperature growth of graphene on metals,[7] or even on dielectric surfaces (550–650 °C).[8] However, without metal catalysts, structural defects readily form at the edges and terminate graphene growth. As a result, small graphene nanoclusters or noncrystalline samples are formed, the quality of which is lower than that required for electrical applications.[8] Vertically oriented graphene nanosheets can be produced by PECVD;[9] however, most of the products are multilayered.

Herein, we describe the development of a critical PECVD (c-PECVD) growth method, in which a H_2 plasma is introduced during graphene growth. H_2 plasma is known to etch graphene from the edges.[10] Moderate etching by a H_2 plasma removes defects generated at the edges and thus keeps the edges atomically smooth and active during the whole process of graphene crystal growth. Therefore, in a critical equilibrium state between H_2 plasma etching and CH_4 or C_2H_4 plasma growth, we observed efficient catalyst-free crystal growth of graphene directly on crystalline sapphire, highly oriented pyrolytic graphite (HOPG), and the amorphous surface of Si substrates with a thermally grown 300 nm SiO_2 overlayer (SiO_2/Si), with crystal sizes up to the micrometer scale for single-layer hexagonal single crystals and up to the centimeter scale for continuous films. The growth temperature could be decreased to as low as 400 °C when C_2H_4 was used as the carbon source. To the best of our knowledge, this temperature is one of the lowest used for the catalyst-free growth of graphene.

In the experiments, a homemade remote radiofrequency (13.56 mHz) PECVD system (80 W) was used (Figure 1a). Figure 1b illustrates the typical procedure for the c-PECVD growth of graphene on bare Si/SiO_2 (see the Experimental Section for details). We first used peel-off graphene to clarify the etching, critical edge growth, and nucleation of graphene in PECVD. Figure 1c shows atomic force microscopy (AFM) images of a trilayer peel-off graphene flake before and after c-PECVD growth (H_2 plasma activation: 250 mTorr, 500 °C; growth: 30 % H_2, 90 mTorr, 600 °C, 60 min). The edges of the bottom, middle, and upper layer moved by 79, 117, and 158 nm, respectively, thus indicating that continuous growth of the flake took place on the edges, rather than in the plane. The different growth rate of each layer is attributed to the substrate (see Figure S1 in the Supporting Information). Control experiments show that the edge growth is highly dependent on the H_2 content, the growth temperature, and the pressure (Figure 1d). Lower temperatures or higher H_2 content tend to induce edge etching, whereas the opposite reaction conditions cause the nucleation of graphitic clusters (see Figure S2). For example, after $CH_4 + H_2$ plasma CVD at a lower temperature (550 °C), instead of growth, the edges of the flakes were etched by about 168 nm (Figure 1e). Upon $CH_4 + H_2$ plasma CVD at a lower H_2 content (20 %), besides the edge growth, small graphitic clusters were nucleated on whole surface of the graphene flakes and SiO_2/Si surface with heights lower than 1 nm (Figure 1f); the heights observed indicate the single-layered nature of the nucleated clusters. The edge growth (Figure 1c; see also Figure S3) only takes place at a well-controlled critical temperature between those needed for nucleation and edge etching, and the critical temperature decreases as the H_2 content decreases (Figure 1d). When C_2H_4 was used as the carbon source in c-PECVD (0 % H_2, 48 mTorr), the critical temperature for edge growth decreased to as low as 400 °C (Figure 1d). Moreover, low pressure can lead to a remarkable improvement in the growth rate. The growth rate (30 % H_2, 600 °C) was about

[*] Dr. D. Wei, Dr. Y. Lu, Prof. W. Chen, Prof. A. T. S. Wee
Department of Physics, National University of Singapore
2 Science Drive 3, Singapore 117542 (Singapore)
E-mail: phyweid@nus.edu.sg
phyweets@nus.edu.sg
C. Han, Dr. T. Niu, Prof. W. Chen
Department of Chemistry, National University of Singapore
2 Science Drive 2, Singapore 117543 (Singapore)

[**] This research was supported by a Lee Kuan Yew Postdoctoral Fellowship (R-144-000-263-112) and AcRF Tier 1 grant (R-144-000-321-112).

Supporting information for this article is available on the WWW under http://dx.doi.org/10.1002/anie.201306086.

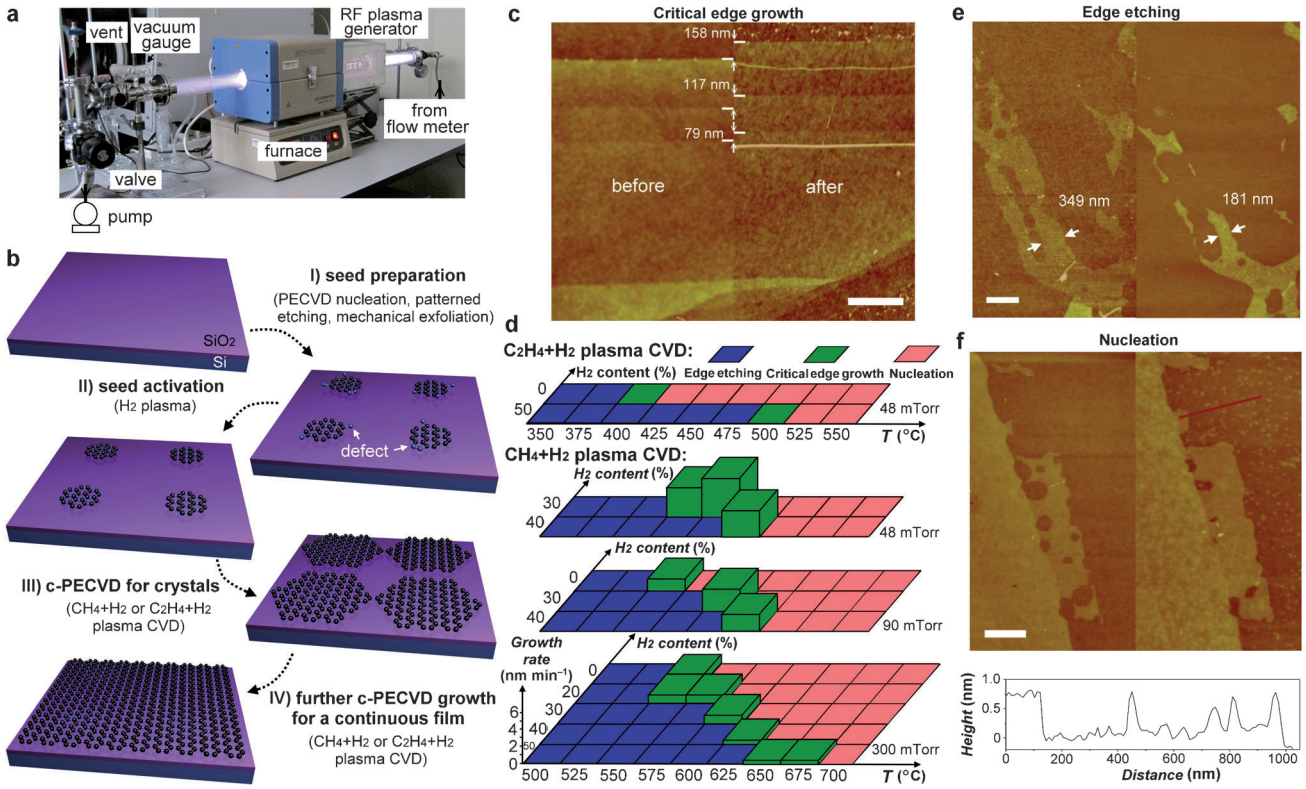

Figure 1. a) The remote radiofrequency (RF) PECVD system used. b) Schematic illustration of the c-PECVD procedure. c) AFM images of a peel-off graphene flake before (left) and after (right) c-PECVD. d) Plots of the experimental results as a function of the temperature (T) and H_2 content at 48, 90, and 300 mTorr. The blue, green, and red areas correspond to the parameters for edge etching, critical edge growth, and cluster nucleation, respectively. The height of the green columns indicates the growth rate. e,f) AFM images of peel-off graphene flakes after activation of the edges with a H_2 plasma (250 mTorr, 500 °C) for 20 min (left columns), followed by $CH_4 + H_2$ plasma CVD (30% H_2, 300 mTorr, 550 °C) for 80 min (e, right column) or $CH_4 + H_2$ plasma CVD (20% H_2, 300 mTorr, 600 °C) for 40 min (f, right column). The height profile across the red line in the AFM image in (f) is shown below the AFM image. Scale bars (c,e,f): 500 nm.

1 nm min^{-1} at 250 mTorr. It significantly increased to about 4.5 nm min^{-1} at 48 mTorr.

We performed scanning tunneling microscopy (STM) studies to clarify the crucial role of the edge in c-PECVD. The samples were prepared on HOPG, which provides an inert conductive surface for both growth and STM analysis. Macrostructural defects were observed on the fresh edges (edge I) of the peel-off HOPG (Figure 2a). Upon H_2 plasma etching (250 mTorr, 500 °C, 30 min), hexagonal holes with neighboring edges (edge II) at an angle of approximately 240° were formed (see Figure S4). No defects were observed in the graphene plane, thus indicating an edge etching mode rather than an in-plane etching mode, in accordance with the Raman results (see Figure S5) and previous studies.[10] On edge II, macrodefects were removed, which resulted in atomically smooth edges, the chirality of which was dominated by the zigzag type (Figure 2b). Although the armchair edge is more stable on an inert surface,[11] previous first-principles calculations revealed that the final edges formed by etching with an H_2 plasma show preferentially a zigzag orientation owing to the more energetically favorable formation of the zigzag configuration in the initial etching stage.[12] Upon $CH_4 + H_2$ plasma CVD (30% H_2, 48 mTorr, 650 °C, 5 min for seed nucleation and 600 °C, 20 min for crystal growth), hexagonal graphene islands with neighboring edges (edge III) at an angle of approximately 120° were formed. STM images revealed that they have a single-crystalline structure with an atomically clean surface (Figure 2c; see also Figures S6 and S7). Both the initial and the newly grown graphene had a defect-free structure, and no defects or boundaries were observed between them (see Figure S7), in accord with the results of Raman spectroscopy (see Figure S8). The edges were atomically smooth, and their chirality was dominated by the armchair configuration, in agreement with previous theoretical studies,[11–13] which predicted that zigzag edges were energetically favorable on Cu,[14,15] whereas the armchair edge has a lower formation energy on an inert surface.

The local electronic density of states near the edge is strongly dependent on the edge structure.[16–19] As a result of the scattering[16,17] and interference[18] of electronic wave functions on a nonuniform edge, complicated STM patterns (see Figure S9) were observed for both edge II and edge III, in which we can identify several typical edge configurations (Figure 2d): zigzag (Z1), armchair (AC11, AC22), and zigzag–armchair (Z-AC), according to the simulated STM patterns (Figure S10) and related studies.[19] Owing to admixing of the zigzag and armchair edges, both the $(\sqrt{3}\times\sqrt{3})R30°$ and honeycomb superstructures were observed (see Figure S11).[16] Moreover, we occasionally observed pentagon–hexagon armchair edges (AC5-6) on edge III. The isolated

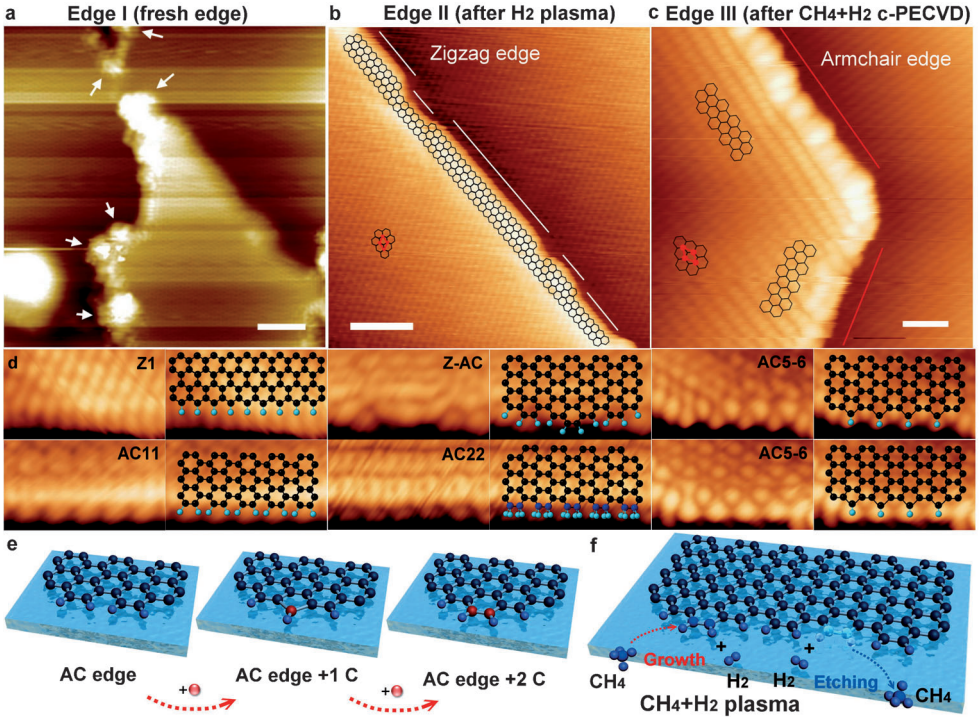

Figure 2. a–c) STM images of the edges after a) mechanical exfoliation (edge I; scale bar: 3 nm; tip bias: 800 mV), b) H_2 plasma etching (edge II; scale bar: 2 nm; tip bias: −600 mV), and c) CH_4+H_2 plasma CVD (edge III; scale bar: 1 nm; tip bias: 800 mV). The arrows in (a) indicate the macrostructural defects. The graphene lattice and a primitive unit cell are marked by black hexagons and a red parallelogram, respectively. d) STM images of several typical edge configurations and the corresponding atomic structures. Black, blue, and cyan balls indicate sp^2 carbon, sp^3 carbon, and hydrogen atoms, respectively. The tip biases are 600 mV (AC11, AC5-6 (bottom image)), 400 mV (Z1), 100 mV (Z-AC), −100 mV (AC22), and −600 mV (AC5-6 (top image)). e) Schematic illustration of edge growth by the sequential addition of two carbon atoms (red) to an armchair (AC) edge (C blue, H cyan). f) Schematic illustration of the reversible equilibrium in c-PECVD.

π electron on pentagon edge atoms can be clearly observed in STM images under both positive and negative tip biases (Figure 2d; see also Figure S12), in contrast to other edge configurations.[13] AC5-6 should be a transition state for catalyst-free growth (see the Supporting Information for details).[11,13]

On transition metals, the metal surface catalyzes the decomposition of organic molecules and reduces the threshold barrier for carbon incorporation;[11] thus, more efficient CVD growth of graphene takes place on metals (800–1000 °C) than on inert surfaces (1100–1650 °C), both energetically and kinetically.[5,6] In this study, the plasma decomposed CH_4 or C_2H_4 molecules into highly reactive C_xH_y species (radicals, ions).[20] This process overcomes the high threshold barrier required for the formation of AC5-6 on inert surfaces when one carbon atom is added and then a lattice hexagon is formed by the incorporation of another carbon atom (Figure 2e).[11,13] Therefore, the catalyst-free growth of graphene on dielectric materials is possible at lower temperatures of 550–675 °C for CH_4+H_2 plasma CVD and 400–500 °C for $C_2H_4+H_2$ plasma CVD. Nevertheless, reactive C_xH_y species are inclined to form structural defects on the edges, and these defects can affect or terminate the crystal growth of graphene. As a result, millimeter-sized hexagonal-monolayer graphene crystals have been grown by CVD on Cu,[15] but pure-CH_4 PECVD typically led to the formation of graphene nanoclusters or noncrystalline samples on inert surfaces.[8] A smooth edge is crucial for catalyst-free graphene growth (macrostructural defects on edge I can terminate the growth). A H_2 plasma can generate H species, which provide moderate etching of the edges but not the graphene plane (Figure 2b)[10] and thus generate atomically smooth edges (edge II). Hence, we need to activate the edges with a H_2 plasma before growth, and also introduce H_2 during PECVD. The reactive H species remove defects generated on edges and thus keep the edges active during the whole growth process. The competition between the effects of H_2 plasma etching and CH_4 plasma growth in c-PECVD (Figure 2f) can be expressed by the following equilibrium:

$$CH_4 \text{ or } C_2H_4\ (g) \underset{\text{etching}}{\overset{\text{growth}}{\rightleftharpoons}} \text{graphene}\ (s) + 2H_2\ (g) - Q$$

in which Q is heat. According to this equilibrium, a high H_2 content or low temperature will cause edge etching; whereas a low H_2 content or high temperature will cause the nucleation of small graphitic clusters, in accordance with the experimental results. There is a critical equilibrium state between these processes in which efficient catalyst-free crystal growth of graphene takes place on the edges to provide larger graphene crystals than those produced by pure-CH_4 PECVD.[8]

Besides peel-off graphene, we also used graphene nanoclusters as the growth seeds (see Figure S13) and produced hexagonal graphene crystals (HGCs) on SiO_2/Si (Figure 3a–d). Small graphitic clusters (Figure 3a) were nucleated on bare SiO_2/Si by CH_4+H_2 plasma CVD at 650 °C (30 % H_2, 48 mTorr, 8 min) and were directly used as seeds for c-PECVD growth at a lower temperature (CH_4+H_2, 30 % H_2, 48 mTorr, 600 °C). After growth for 90 min, HGCs were distributed on the whole substrate (Figure 3b; see also Figures S14–S16). Figure 3e shows a typical transmission electron microscopy (TEM) image of a HGC. The same set of sixfold-symmetric diffraction spots, which correspond with

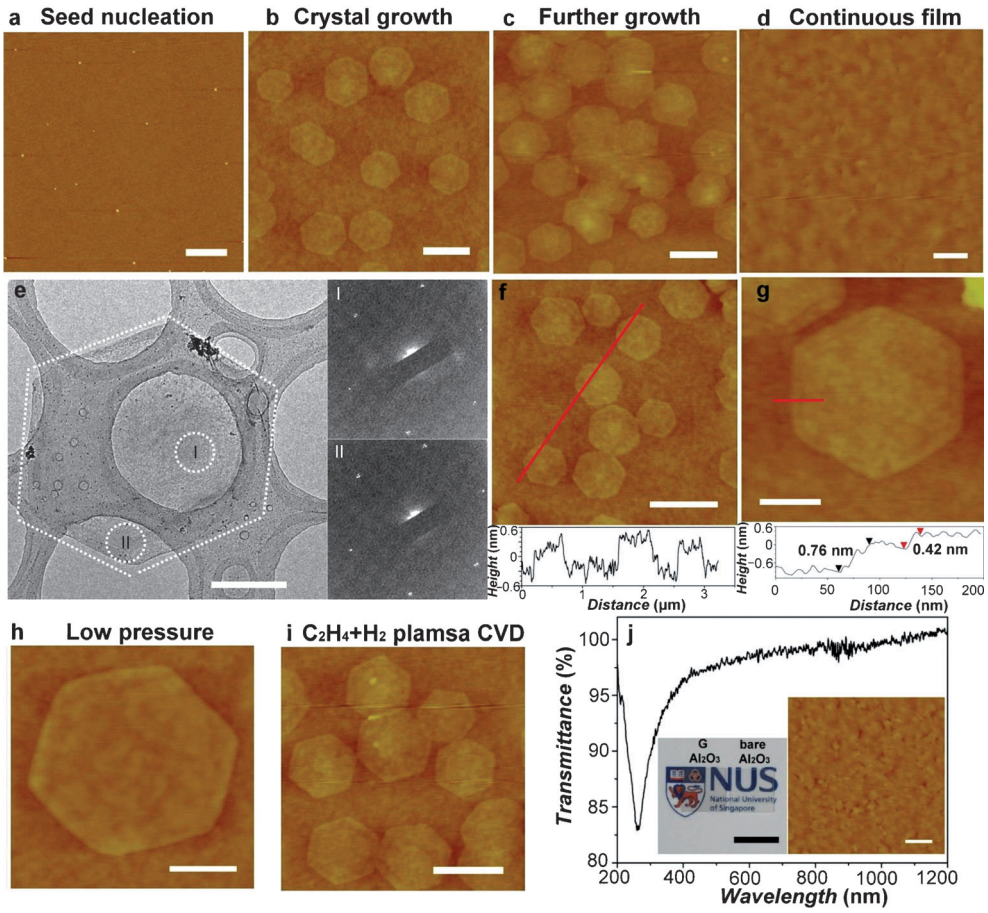

Figure 3. a) AFM image of the graphitic clusters after nucleation at 650 °C. b,c) AFM images of the HGCs on SiO_2/Si after c-PECVD (CH_4+H_2) growth at 600 °C for 90 min (b) and for 120 min (c). d) AFM image of a graphene membrane on SiO_2/Si. e) TEM image of a HGC highlighted by dashed lines. The two images on the right are selected-area electron diffraction patterns for the regions indicated by dashed circles. f,g) AFM images of single-layer HGCs (f) and a bilayer HGC (g) grown by c-PECVD (CH_4+H_2). The height profiles across the red lines are shown below the AFM images. h) AFM image of a HGC grown by c-PECVD (CH_4+H_2) at 48 mTorr on SiO_2/Si. i) AFM image of HGCs grown by c-PECVD ($C_2H_4+H_2$) at 48 mTorr on SiO_2/Si. j) Transmittance spectrum of a graphene film grown on a sapphire substrate by c-PECVD (CH_4+H_2, 30% H_2, 48 mTorr, 650 °C, 12 min for nucleation and 600 °C, 150 min for growth). Insets: photograph (scale bar: 1 cm) and AFM image (scale bar: 1 μm) of the graphene film. Scale bars: a–c,f,i) 1 μm, d) 2 μm, e,g) 250 nm, h) 500 nm.

that of a graphene crystal with armchair edges,[14] were observed at different locations, thus confirming the single-crystalline nature of the sample. Owing to the random nucleation of the seeds, the resulting HGCs were oriented randomly. Most HGCs had a single-layer structure (Figure 3 f). Bilayer or trilayer graphene crystals were occasionally observed (Figure 3 g; see also Figures S17 and S18). The narrow strong 2D band in the Raman spectrum (see Figure S19) confirms their single-layer structure.[21] The weak D band is attributed to the armchair edges of HGCs.[22] Further c-PECVD growth enlarged the size of the grains (Figure 3 c; see Figures S20 and S21) and linked neighboring grains together, which finally resulted in a continuous graphene film on SiO_2/Si (Figure 3 d).

Low pressure favors crystal growth. At lower pressure, the reduced scattering in the plasma leads to both increased density and increased impact energy of C_xH_y species, which probably result in promotion of the graphene growth.[20] HGCs with sizes as large as 1.35 μm (Figure 3 h) were produced at a pressure of 48 mTorr (30% H_2, 600 °C, 180 min). Moreover, as compared with CH_4+H_2 plasma CVD, $C_2H_4+H_2$ plasma CVD led to the nucleation and c-PECVD growth of HGCs at a lower temperature. HGCs with sizes up to 1.2 μm (Figure 3 i) were produced on SiO_2/Si by nucleation at 450 °C (100% C_2H_4, 5 min) and growth at 400 °C (100% C_2H_4, 160 min). We also prepared continuous graphene films on sapphire substrates (Figure 3 j; see also Figure S22), which had sheet resistance of $4.1\times10^3\,\Omega\,sq^{-1}$ and a transmittance of 97.6% at 550 nm. Another route for the preparation of the graphene seeds is patterned etching (see Figure S23). An array of graphene seeds were produced by oxygen plasma etching of a peel-off flake by the use of a poly(methyl methacrylate) (PMMA) mask patterned by electron-beam lithography (EBL). After H_2 plasma activation and c-PECVD, well-arrayed HGCs were produced on SiO_2/Si with uniform sizes and orientations. These results show the high reliability and controllability of c-PECVD for graphene-crystal growth.

One benefit of c-PECVD is that it provides high-quality graphene (G) samples with atomically clean surface on dielectric materials, which can be directly used in high-performance electrical devices. As an example, we fabricated field-effect transistors (FETs) by using HGCs. As the growth substrate, SiO_2/Si was used as the dielectric material and the bottom gate (Figure 4 a,b; see also Figure S24). The devices were current-annealed (see Figure S25) in a vacuum to remove the absorbed molecules[23] and were then analyzed in a vacuum (7×10^{-8} mbar) at room temperature. The symmetrical linear output curves (Figure 4 c) indicate ohmic contacts between the HGC and the electrodes. Owing to p-type doping of the HGC by the Au/Cr contact,[24] the transfer curve (Figure 4 d) shows a Dirac point at a positive gate voltage (typically 10–30 V). Calculated FET mobilities are in

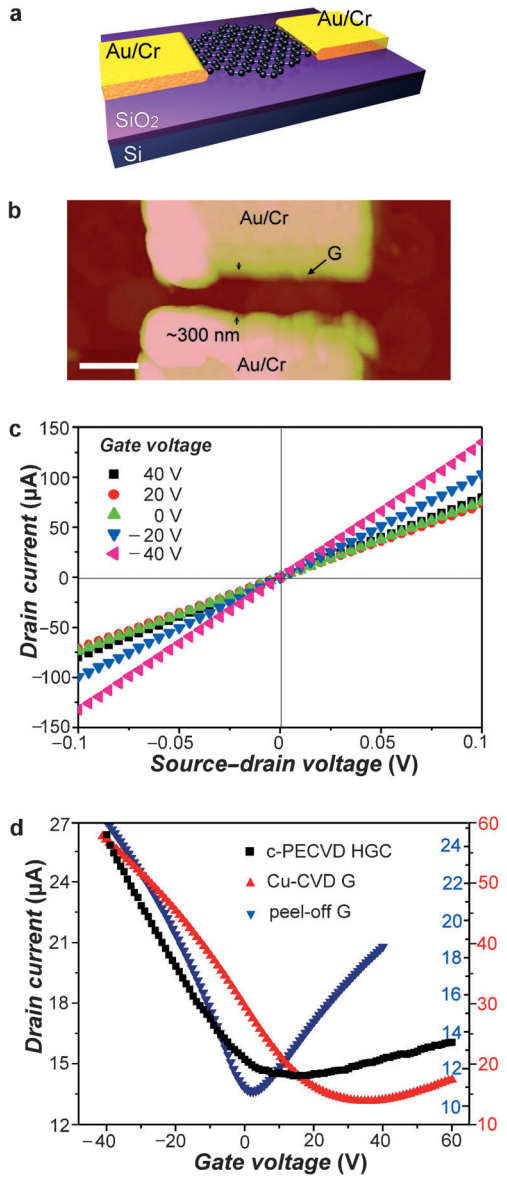

Figure 4. a) Bird's-eye view of a schematic device configuration. b) AFM image of the device (scale bar: 500 nm). c) Output characteristics of the FET device. d) Transfer characteristics (source drain voltage: 0.02 V) of FET devices with HGC (black), Cu-CVD graphene (red), and peel-off graphene (blue).

the range of 550–1600 $cm^2V^{-1}s^{-1}$. For comparison, when FETs of Cu-CVD graphene (see Figure S26) and peel-off graphene (see Figure S27) were fabricated and analyzed under the same conditions, they showed mobilities in the range of 600–1500 $cm^2V^{-1}s^{-1}$ and 850–2200 $cm^2V^{-1}s^{-1}$, respectively. We believe that the device mobility can be further increased by improving the technical aspects of device fabrication, for example, by decreasing the contact resistance and by the use of substrates other than SiO_2 to reduce the amount of charged impurities trapped on the substrate.[25] The comparable mobility of the HGCs to those of both graphene materials prepared by Cu-CVD and peel-off graphene materials indicates their high electrical quality for device applications.

In conclusion, we observed a critical equilibrium state of graphene edge growth in CH_4+H_2 and $C_2H_4+H_2$ plasma CVD. On the basis of this finding, we developed a c-PECVD method for the production of micrometer-scale graphene crystals directly on dielectric substrates at temperatures as low as 400 °C. The resulting materials can be directly incorporated into electronic devices, thus avoiding the post-growth transfer process that is normally required. The avoidance of such a transfer step as well as the high controllability of the process, the high quality of the graphene produced, and the compatibility of this method with current microelectronics make this approach a promising growth method for future graphene electronics.

Experimental Section

A SiO_2/Si or sapphire substrate was cleaned and then annealed in H_2 (99.9995 %; 50 mTorr) at 1000 °C for 15 min to produce a clean substrate. Three kinds of seeds were prepared on the substrate for graphene growth: 1) peel-off graphene produced by mechanical exfoliation with scotch tape; 2) graphitic clusters nucleated by CH_4 (99.9 %) + H_2 plasma CVD (30 % H_2, 48 mTorr, 650 °C) or C_2H_4 (99.9 %) + H_2 plasma CVD (50 % H_2, 48 mTorr, 550 °C); 3) graphene nanoislands patterned by EBL and oxygen plasma etching. The substrate with the seeds was then placed in the center of a furnace, and a H_2 plasma (H_2: 250 mTorr) was generated upstream by a radiofrequency plasma generator (K-Mate, VERG-500) to activate the edge of the seeds at 500 °C. CH_4+H_2 plasma CVD (30 % H_2, 48 mTorr, 600 °C) or $C_2H_4+H_2$ plasma CVD (50 % H_2, 48 mTorr, 500 °C) was then used for the growth of graphene. In the steps in which a plasma was used, the plasma flame filled whole quartz tube, which resulted in high efficiency of plasma etching or growth. Finally, the furnace was cooled to room temperature in H_2 (50 mTorr) after the growth step. The as-grown samples were analyzed by AFM (Veeco D3000; tapping mode), field-emission SEM (JEOL JSM-6700F), field-emission TEM (JEOL 2010F; acceleration voltage: 200 kV), Raman spectroscopy (Alpha 300R, 514 nm), and STM. Electrical characterization was carried out in a vacuum (7×10^{-8} mbar) at room temperature by the use of a semiconductor analyzer (Agilent B2912A; see the Supporting Information for details).

Received: July 12, 2013
Revised: September 18, 2013
Published online: October 31, 2013

Keywords: chemical vapor deposition · crystal growth · graphene · nanomaterials · scanning probe microscopy

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